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INSTITUTE OF ENERGY CONVERSION

UNITED STATES DEPARTMENT OF ENERGY
UNIVERSITY CENTER OF EXCELLENCE
FOR PHOTOVOLTAIC RESEARCH AND EDUCATION

September 21, 2007

Bolko von Roedern
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

Re: NREL Subcontract #ADJ-1-30630-12
D.5.20

Dear Bolko,

This report covers research conducted at the Institute of Energy Conversion (IEC) for the period of June 1, 2007 to June 30, 2007 under the subject subcontract. The report highlights progress and results obtained under Task 1 (CdTe-based solar cells).

Task 1 - CdTe-based Solar Cells

Summary

In this report, issues related to high throughput processing of and junction-limiting factors in thin film CdTe solar cells are reported. Concerns over possible sources of impurity contamination of CdTe has prompted further analysis of the influence of soda lime glass (SLG) SLG/SnO_2 substrate preparation as well as the chemistry of the CdS growth and its effect on the CdS-CdTe junction region. With respect to high throughput deposition and CdTe usage, we have deposited CdTe films by VT with sub-micron thickness having low pinhole density.

Effects of Glass/TCO

Based on the results in the previous report, evaluating baseline transparent conductive oxide (TCO) processing for CdTe/CdS thin film cells with vapor transport CdTe, we continued with the study of uncontrolled impurities originating in the TEC 15 SLG/SnO_2 substrate. We examined variability of the TEC 15 itself be comparing devices with identical processing but using different batches of glass/SnO_2. We also continued to look at ways to remove or bury the impurities from the glass and SnO_2 prior to any deposition by varying Ga thickness and adding an ITO barrier layer. The variations in TEC 15 SLG/SnO_2 substrate preparation are listed in Table I.

Table I. Window layer processing procedures for 4 baseline CdTe depositions

Run Number	TEC 15 batch	Diffusion barrier	ED Ga Deposition Time (min.)	CdS Processing
272	current	none	15.0	
276	current	2200 Å ITO	12.5	
277	current	2200 Å ITO	12.5	Etch ½ CdS
278	2-year old	none	12.5	

One of the variations listed in Table I was the TEC 15 TCO batch received from the supplier. We made a direct comparison of the TCO from our current supply to a piece saved from a batch we received two years ago. The substrates were cleaned using our standard Crest cleaning system consisting of a 65°C ultrasonic soap (Liquinox) wash, followed by a de-ionized water rinse done in our standard Crest cleaning system ultrasonic tank. The water rinsed samples were then dried in a forced hot air dryer. A couple of substrates were coated with 220 nm thick ITO, deposited by rf sputtering. All samples then received an ED Ga coating and were oxidized for 15 minutes at 550°C after cleaning. Following the oxidation step, all the samples received our baseline CdS and CdTe film deposition. In one case (VT 277), half of the CdS film was immersed in glacial acetic acid for 1 minute; this is a selective etchant for the native oxide $CdSO_4$. Cells were processed with the established baseline vapor $CdCl_2$ treatment for 2 minutes at 480°C and aniline treatment, with Cu/Ni contacts. The best cell results are listed in Table II.

Table II. Cell results for different window layer processing.

Plate and Cell Number	TEC 15 batch	Diffusion barrier	Ga dep (min)	CdS Etch	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)
272.1-7	current	none	15.0	N	755	24.2	65.9
276.2-3	current	ITO	12.5	N	526	17.1	45.3
277.1-6	current	ITO	12.5	Y	582	23.2	52.6
277.2-4	current	ITO	12.5	N	583	22.5	44.7
278.1-1	2-year old	none	12.5	N	704	25.5	65.2

Cells made with no special processing, and with old and new batches of TEC 15 TCO exhibit comparable performance. The device with longer Ga deposition (VT272) has slightly higher V_{OC}. The addition of an ITO layer to the TCO prior to Ga_2O_3 (VT 276 and VT 277) yielded lower V_{OC}, J_{SC} and FF. Thus, adding an ITO barrier coating had the unexpected effect of reducing V_{OC} and FF. The additional etch of CdS in glacial acetic acid prior to CdTe deposition did not affect the V_{OC} and marginally improved the other parameters. Follow-up trace impurity analysis in these films and in previous films without Ga_2O_3 layers is planned.

CdS Deposition

The baseline IEC CdTe cell process utilizes CdS deposited by chemical surface deposition (CSD) in a three-step process. A detailed investigation of the CdS growth and materials properties is being carried out to isolate potential effects on device operation and cell performance. Using measured optical absorption in the high absorption regime of CdS (400 nm), each coat of CSD CdS is found to add ~40 nm. Thus, the growth is linear with time, corresponding to a rate of 8 nm per minute. The baseline process also utilizes a thermal treatment in $CdCl_2$ vapor and air. This treatment does not alter the measured thickness of CdS but changes other properties, particularly the surface composition.

Atomic force microscopy was used to analyze the morphology of the terminating surface of the CdS film. The r.m.s. surface roughness and size of CdS features were insignificantly changed by increasing film thickness or heat treatment. This is consistent with the conformal growth offered by the CSD process. Glancing incident x-ray diffraction (GIXRD) analysis indicates that the CdS film exhibits hexagonal structure (Figure 1). The strongest reflections belong to the (110) and (002) planes. After the heat treatment, all peaks sharpened, indicating a high degree of crystallization after heat treatment. Three additional reflections appear: CdS (100), (101) and (110) and films become more randomly oriented after the treatment. This is verified by the calculation of orientation parameters of different CdS planes. For all three samples, the parameters calculated are much closer to 1 after the heat treatment, indicating random orientation. Note that although GIXRD with two-circle goniometer cannot be used to accurately assess preferred orientation, it does permit verification of random orientation. From this result and that of grain size described above, it can be concluded that the orientation within the grains are rearranged, but the grain size does not change much, so the heat treatment has enough energy to cause the primary recrystallization but not grain coalescence. The tetragonal SnO_2 film was unchanged by the heat treatment.

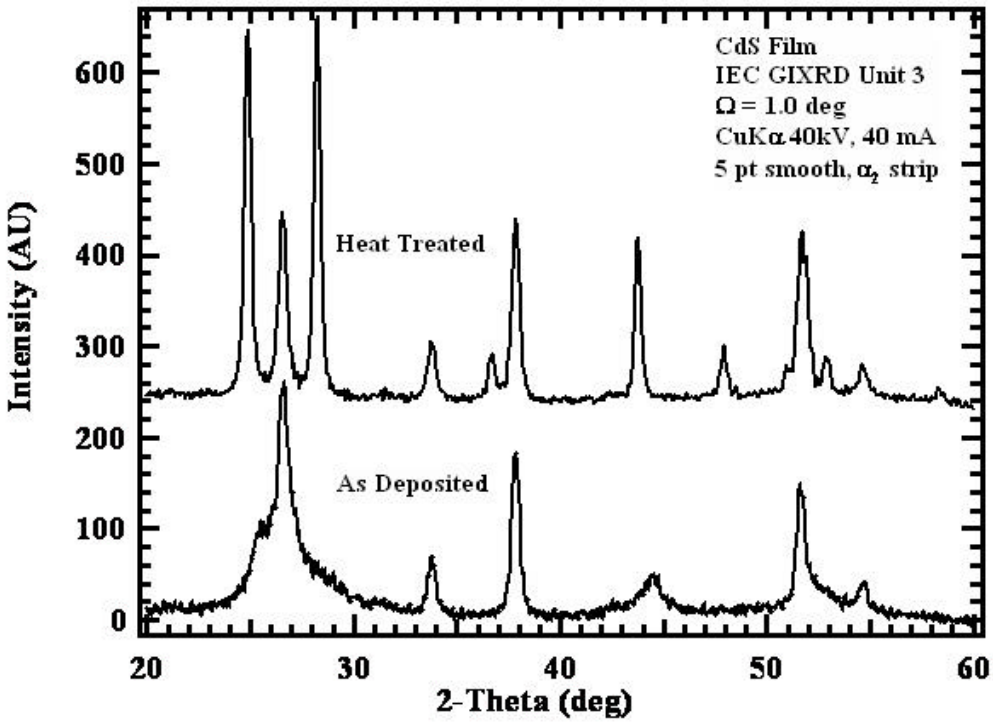

Figure 1. GIXRD (1 deg incidence) of CdS/SnO_2/SLG before and after $CdCl_2$ vapor treatment.

With increasing CdS thickness, the average optical transmission between 500nm (2.49eV) and 900nm (1.38eV) decreased from 90% (no CdS) to 82% (3 coats) (Figure 2). After heat treatment, the average film transmission in the red increased by approximately 1% and the transmission edge sharpened, consistent with enhanced crystallinity after the heat treatment. A linear relation between $(ah?)^2$ and h? shows that as-deposited CdS is a direct band gap material with extrapolated band gap energy E_G = 2.50eV. After $CdCl_2$ heat treatment, the band gap decreased to about 2.40eV, close to the accepted value for single crystal CdS.

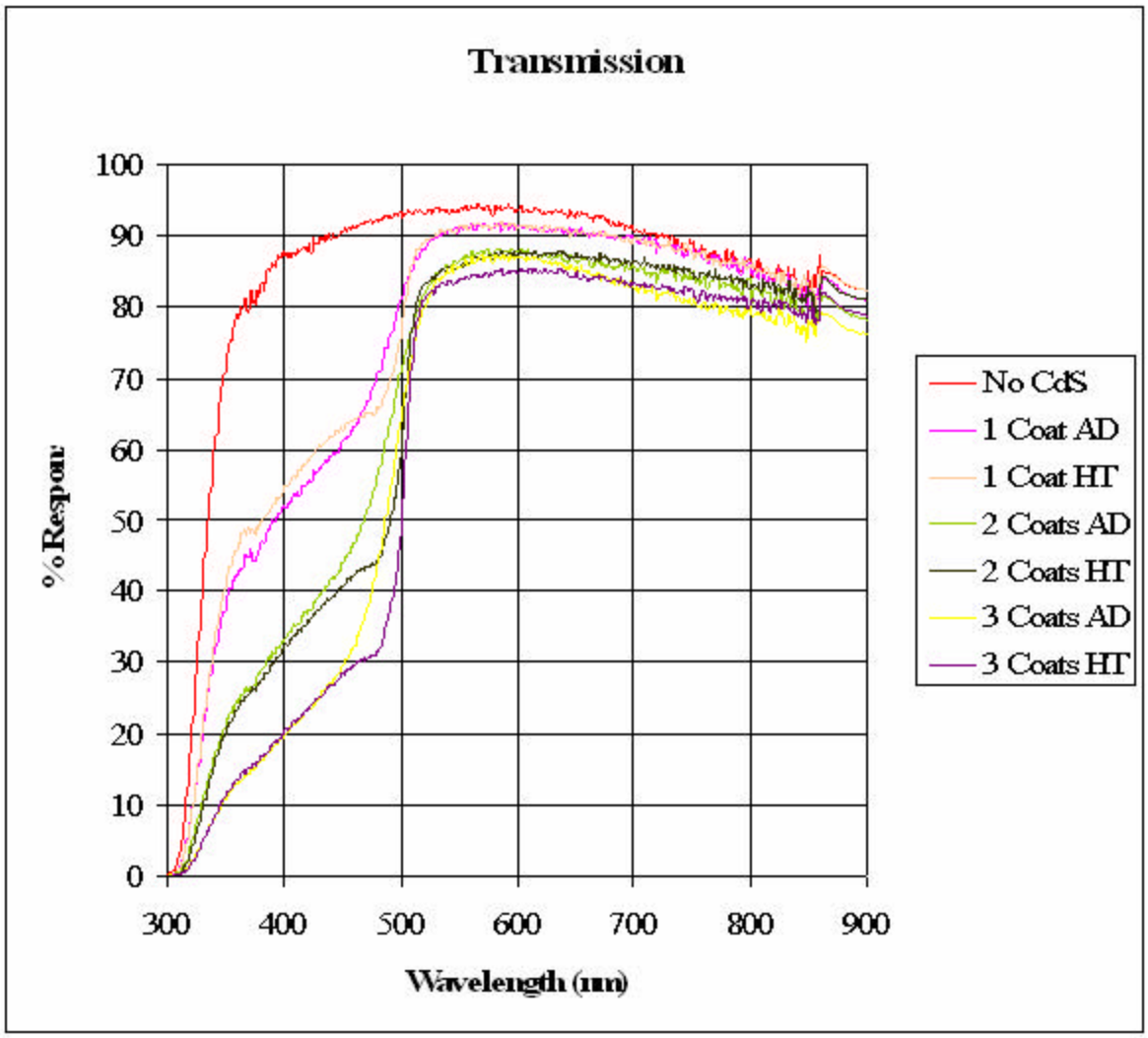

Figure 2. Optical transmission of CdS films deposited by CSD onto SLG/SnO_2 after deposition (AD) and $CdCl_2$ vapor heat treatment (HT).

X-ray photoemission spectroscopy (XPS) analysis was carried out on the sample receiving three coats of CdS. The atomic concentrations of deposited thin film showed that S/Cd = 1: 0.62, S/O = 1: 0.58, and S/C = 1: 0.97 indicating that the surface is sulfur rich. After heat treatment, the results were S/Cd = 1: 0.64, S/O = 1: 1.86, and S/C = 1: 5.31 indicating that the ratio of S to Cd stays the same before and after $CdCl_2$ heat treatment, while oxygen and carbon increased significantly. Further work is planned to examine the depth profile of composition, and the effects of surface treatment: 1) vacuum heat treatment to desorb excess oxygen, sulfur, carbon, etc., and 2) acetic acid etch treatment to remove compounds such as $CdSO_4$.

High Throughput Processing

Exploratory vapor transport depositions in other growth regimes than baseline are being conducted to facilitate deposition of dense pinhole-free CdTe films with sub-micron thickness. According to the VT growth model, several methods can be employed to reduce thickness: 1)

increase translation speed; 2) decrease source temperature and linear flow velocity through the source; and 3) raise total system pressure. Baseline deposition of 6-7 micron thick films is carried out at a source temperature of 850°C, total pressure of 20 Torr, and flow rate of 20 sccm in N_2 carrier gas and N_2:O_2 ambient. We have found that decreasing source temperature is not easily controlled and the carrier gas can become under-saturated, which yields non-uniform deposits. Increasing translation speed has yielded films with good thickness control and uniformity but with excessive pinholes. During this period, depositions were carried out at higher pressure, 100 Torr and lower flow rate, 2 sccm. For a weakly reactive carrier gas, such as N_2:O_2, these conditions are expected to increase doping effects from CdTe-gas interactions than at lower pressure. The obtained films were 0.7 micron thick and exhibited very low pinhole density and good uniformity. The improved quality of the deposit is attributed to uniform reduction of growth rate, obtained by increasing diffusion kinetics within the source. Results of the solar cells will be reported later.

V_{OC} and Junction Operation

Since one of the goals of this project is to provide insight into limitations to obtaining high Voc, we have analyzed the dark JV curves to obtain recombination current JO and A-factor on devices with a wide range of V_{OC}. The commonly reported V_{OC} relation is,

$$V_{OC} = AkT/q [\ln (J_L/J_O] \quad (1)$$

with

$$J_O = J_{OO} \exp (\phi/AkT), \quad (2)$$

where J_L is the light generated current (J_L is reduced by voltage dependent collection and is typically half of J_{SC} near open circuit, reducing V_{OC} by about 20 mV), J_{OO} is the recombination current density, ϕ is the barrier height (typically the band gap for Shockley Read Hall recombination) and A is the diode factor. ϕ/A is the activation energy for the recombination mechanism. From Equations 1 and 2, the open circuit voltage V_{OC}

$$(V_{OC} / A) = kT/q [\ln (J_L/J_O] = \phi/(qA) – kT/q \ln (J_{OO} / J_L). \quad (3)$$

Figure 3 shows log J vs. V_J for three devices from their dark J-V curve. Two are listed in Table II and device VT249.1 processed in 2006 and having V_{OC}=0.799 V, J_{SC}=24.4 mA/cm^2 and FF=70%. It is included as an example with high V_{OC} relative to recent devices. The external voltage V is related to the actual voltage across the internal junction V_J by correcting for the series resistance R_S. Values of A and J_O obtained from the data are listed in the figure. As expected, the device with the highest V_{OC} has the lowest J_O and vice versa. Figure 4 shows V_{OC} and V_{OC}/A vs. log of the dark J_O for 5 recent devices plus VT249.1. V_{OC} ranges from 0.52 to 0.80 V. All devices had A=1.5-2.0 except for the one with the lowest V_{OC} (A=3.5 indicating non-SRH recombination). Note the generally poor correlation between V_{OC} and J_O but the excellent correlation between V_{OC}/A and J_O. We use the dark J_O because obtaining J_O from the light J-V curve is problematic due to voltage dependent collection. The close correlation confirms that the dark J_O is relevant to the V_{OC} after correction for variations in A. Using Eq 3

with ϕ = 1.5 eV and J_L=12 mA/cm^2, we obtain $J_{OO} = 10^8 – 10^{12}$ mA/cm^2 after excluding the device with A=3.5. Various models for J_{OO} exist but temperature-dependent J-V measurements would be needed to identify which one was applicable. However, decreasing the lowest J_{OO} by a factor of 10 with the same A=1.5 would increase V_{OC} from 0.79 to 0.88 V.

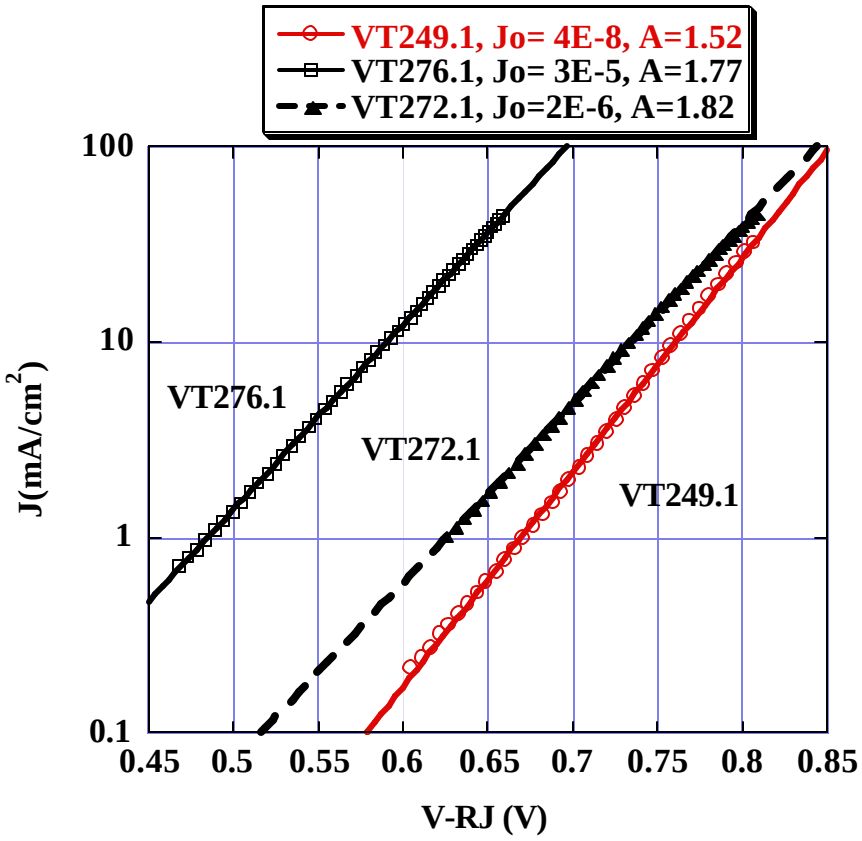

Figure 3. Log J vs. corrected V for 3 devices having V_{OC} values of 0.62 V (VT276.1), 0.75 V (VT272.1) and 0.80 V (VT249.1). Values of J_O (mA/cm^2) and A extracted from the intercept and slope.

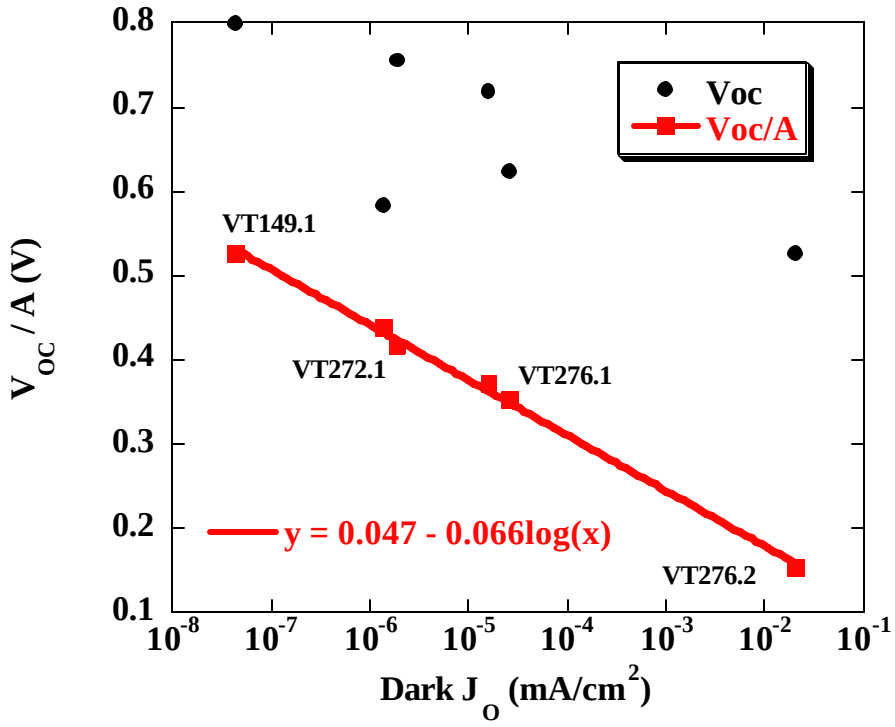

Figure 4. V_{OC} (black circles) or V_{OC}/A (red squares) vs. log dark J_O for 6 recent devices having V_{OC} from 0.52V to 0.80V.

Best regards,

Robert W. Birkmire
Director

cc: Paula Newton, IEC
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